AMENDMENTS TO THE CLAIMS

1. (Currently amended) A control apparatus for operating with program data, the apparatus comprising:

a first memory for storing program data;

a second memory for storing program data;

a writing means for writing data in the second memory;

a first selection means for selectively outputting an output from one of the first and second memories;

a control means for outputting a first address to one of the first and second memories and operating in accordance with program data output from the first selection means;

the first selection means selecting the output from one of the first and second memories in accordance with the first address;

the writing means enabling data to be written in the second memory when the control means is operating in accordance with the program data from the first memory;

a system controller for outputting program data to the writing means and a second address for the second memory when the control means is operating in accordance with the [[data]] program data from the first memory; and

a second selection means for selectively outputting an address for the second memory from one of the control means and the system controller;

the second selection means selecting the second address form the system controller when the control means is operating in accordance with the [[date]] program data from the first memory.

2. (Currently amended) The control apparatus according to claim 1, wherein the control means includes a read address generation means for generating the first address for reading one of the first and second ~~memory~~ memories, the read address generation means generating the first address so as to select the output from one of the first and second ~~memory~~ memories in accordance with the program data.

3. (Currently amended) A control apparatus for operating with program data, the apparatus comprising:

a first memory for storing program data;

a second memory for storing program data;

a writing means for writing data in the second memory;

a first selection means for selectively outputting an output from one of the first and second memories;

a control means for outputting a first address to one of the first and second memories and operating in accordance with program data output from the first selection means;

a parameter memory that can store a parameter therein;

the first selection means selecting the output from one of the first and second memories in accordance with the parameter;

the writing means enabling data to be written in the second memory when the control means is operating in accordance with the program data from the first memory;

a system controller for outputting program data to the writing means and a second address for the second memory when the control means is operating in accordance with [[data]] program data from the first memory; and

a second selection means for selectively outputting an address for the second memory from one of the control means and the system controller;

the second selection means selecting the second address from the system controller when the control means is operating in accordance with the [[data]] program data from the first memory.

4. (Currently amended) The control apparatus according to claim 3, and further comprising a read address generation means for generating the first address for reading [[on e]] one of the first and second ~~memory~~ memories, the read address generation means generating the first address so as to select the output from one of the first and second ~~memory~~ memories in accordance with the parameter stored in the parameter memory.

5. (Previously presented) The control apparatus according to claim 2, wherein the writing means includes a write address generation means for generating an address to be written in the second memory, the writing means switching the output from the read address generation means and the output from the write address generation means in accordance with the output from the read address generation means and outputting the selected output to the second memory.

6. (Previously presented) The control apparatus according to claim 4, wherein the writing means includes a write address generation means for generating an address to be written in the second memory, the writing means switching the output from the read address generation means and the output from the write address generation means in accordance with the output from the read address generation means and outputting the selected output to the second memory.

7. (Previously presented) The control apparatus according to claim 1, wherein a program is configured to arbitrarily switch the output from the first memory and the output from the second memory as program data.

8. (Previously presented) The control apparatus according to claim 3, wherein a program is configured to arbitrarily switch the output from the first memory and the output from the second memory as program data.

9. (Currently amended) The control apparatus according to claim 1, wherein one of the first and second ~~memory~~ memories is a one-chip semiconductor element.

10. (Currently amended) The control apparatus according to claim 3, wherein one of the first and second ~~memory~~ memories is a one-chip semiconductor element.

11. (Previously presented) The control apparatus according to claim 1, wherein the second memory is a SRAM.

12. (Previously presented) The control apparatus according to claim 3, wherein the second memory is a SRAM.

13. (Currently amended) A control apparatus for operating with program data, the apparatus including a one-chip semiconductor element comprising:

a first memory that is read only for storing program data;

a second memory that allows write and [[read]] read, for storing program data;

a writing means for writing data in the second memory;

a first selection means for selectively outputting an output from one of the first and second memories;

a control circuit for control operation in accordance with the output from the first selection means;

the control apparatus enabling data to be written in the second memory while the control circuit is performing control operation in accordance with the program data from the first memory;

a system controller for outputting program data to the writing means and a second address for the second memory when the control circuit is operating in accordance with [[data]] program data from the first memory; and

a second selection means for selectively outputting an address for the second memory from one of the control ~~means~~ circuit and the system controller;

the second selection means selecting the second address from the system controller when the control ~~means~~ circuit is operating in accordance with the [[data]] program data from the first memory.

Claims 14-16 (Cancelled)

17. (Previously presented) The control apparatus according to claim 2, wherein the writing means includes a write address generation means for generating the second address to be

written to in the second memory, the writing means selecting from between the first address and the second address in accordance with the first address and providing the selected address to the second memory.

18. (Previously presented) The control apparatus according to claim 4, wherein the writing means includes a write address generation means for generating the second address to be written to in the second memory, the writing means selecting from between the first address and the second address in accordance with the first address and providing the selected address to the second memory.